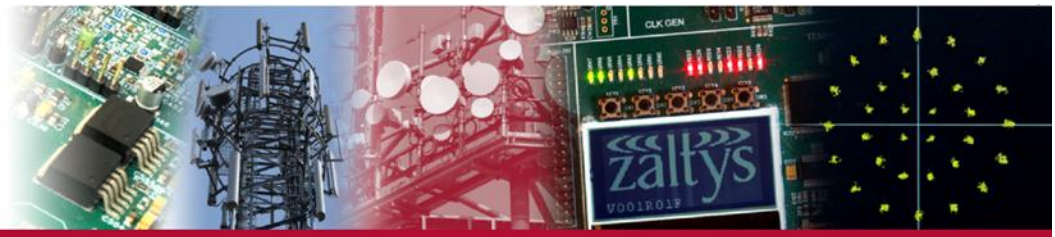


ISDB-T Modulator Core ISDBT-M

Introduction

The Zaltys ISDBT-M IP core is a 3-layer ISDB-T hierarchical modulator compatible with the ARIB STD-B31 standard for Terrestrial Integrated Services Digital Broadcasting. The core can process either a single BTS transport stream (containing information for all three layers of the ISDB-T frame structure), a single MPEG transport stream (with user assigned mapping of PID's to layers), or three independent MPEG transport streams, one for each layer. It performs all the necessary processing required to output a complex modulated baseband signal to a pair of external DACs.

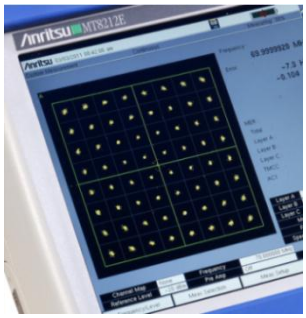
The bandwidth of the generated signal is directly related to the supplied system clock, as per the table below. One sample is sent to the external DACs every eight system clock cycles.

Transmission Bandwidth	System Clock Frequency
6 MHz	4096 / 63 (65.01587…) MHz
7 MHz	2048 / 27 (75.85185…) MHz
8 MHz	16384 / 189 (86.68783…) MHz

An external DDR2 SDRAM device is required to support the BTS interface, time interleaving, and 2 or 3-layer operation. The device should be compatible with a Micron MT47H32M16 512Mbit DDR2 SDRAM (8M x 16 bit x 4 banks).

Applications

The ISDBT-M core is ideally suited to applications such as broadcast digital television, mobile television cameras, and outside broadcast units.



64QAM ISDB-T Constellation at modulator output

Features

- Full 13-segment ISDB-T modulator
- ARIB STD-B31 compliant operation, supporting one, two or three-layers
- Flexible transport-stream input interface
  - Single BTS input, or
  - Single TS input with layer mapping, or
  - Individual TS inputs for each layer
- Test-mode traffic generator
- Microprocessor controllable
- Fully synchronous design
- Available now for Xilinx FPGA

Technical Overview

A single BTS transport stream can be input to the core, carrying all the information necessary to construct a full 3-layer ISDB-T baseband signal as per ARIB STD-B31. Alternatively, if single-frequency network operation is not required, a single combined TS stream can be divided and mapped to each layer, or alternatively three separate TS streams can be accepted and fed independently to each layer. Settings for modulation scheme, FEC code rate, & time-interleaver depth are individually applied to each layer, before the resulting data is frequency-interleaved. Pilot carriers are then added, along with TMCC and AC information. The resulting 13-segment frame is then passed through an IFFT block, and a programmable guard interval is copied into the result before being sent to the external I & Q DACs.

Tokyo's NTC Tower

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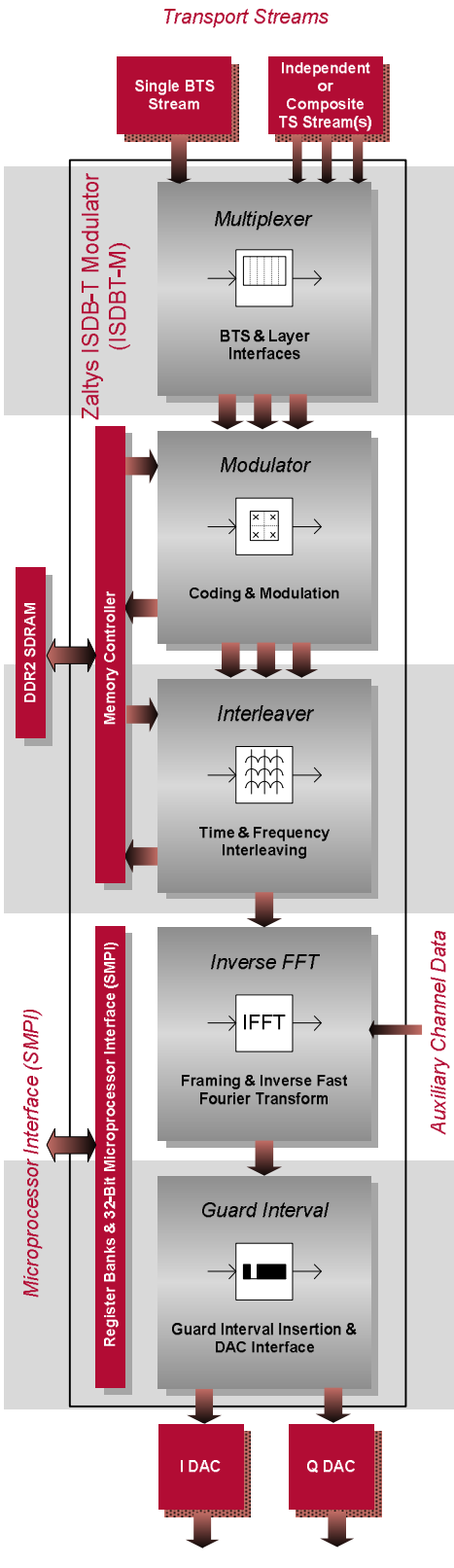
ISDB-T Modulator Core



Technical Overview continued

A single Broadcast Transport Stream (BTS), formatted according to ARIB STD-B31, can be decoded and used to drive data into all 3 layers of the ISDB-T framing structure. A time delay of up to one second can be applied to the incoming BTS stream to allow alignment with other transmitters in a single-frequency network (SFN). Alternatively, for non-SFN use, either a single composite TS or three independent TS streams may be accepted and routed to each of the layers.

The Modulator block is replicated for each layer. It takes the MPEG packets and adds a Reed Solomon outer code, followed by energy dispersal, delay adjustment and byte wise interleaving. It then adds a convolutional inner code, with each layer having its own unique code rate. Further delay adjustment is applied before performing a bit-interleave operation and mapping the resulting data to I & Q constellation points, with each layer having its own unique modulation, coding, and interleave settings.

Each layer is assigned a single or group of segments to transport it. The segments corresponding to each layer are time-interleaved according to the depth parameter for that particular layer. The segments are then split into portions depending on whether they are associated with partial reception, coherent modulation, or differential modulation. Each individual segment corresponding to the differential and coherent portions is then frequency-interleaved within itself. The individual groups of segments corresponding to partial reception, coherent modulation, or differential modulation are then frequency-interleaved within themselves by performing a carrier rotation followed by a carrier randomisation.

The interleaved data is combined with pilot tones, TMCC information, and the AC channels to form the OFDM segment frame. The frame makeup differs depending on whether differential or coherent modulation is present in the segment. The 13-segments are then ordered, a continual pilot tone is added to the higher edge of the band, and the whole configuration is sent to a complex 2K, 4K or 8K IFFT to generate the OFDM symbols.

After the IFFT, a guard interval is inserted into the data stream by concatenating samples copied from the end of the IFFT result onto the front of the IFFT result. The final output takes the form of I & Q sample pairs suitable for passing to a pair of 16-bit DACs.

Deliverables

There are three licensing models for this IP core (each with a royalty-free and a royalty-based variant):

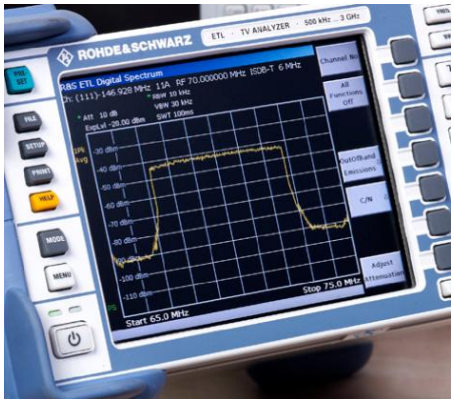
- Single-Project Netlist (project-based, Xilinx-specific)
- Multi-Project Netlist (site-based, Xilinx-specific)
- Multi-Project VHDL (site-based, source-code)

Deliverables	
Design Formats	Xilinx technology specific netlist VHDL source (source-code licences only)
Documentation	Hardware & programming guide
Constraints	FPGA constraints guide file
Verification	VHDL verification testbench
Templates	VHDL & verilog instantiation templates

Support
3 months support included

Applications

- Professional ISDB-T broadcast transmitters
- Professional test and measurement equipment
- TV head end, up-link and down-link equipment
- Multi-Dweller Unit and residential distribution equipment
- Point-to-point hierarchical communications



ISDB-T Spectrum at modulator output

Full Features List

- Full 13-segment ISDB-T modulator, supporting 1, 2 or 3 (hierarchical) layers and compliant with the ARIB STD-B31 standard
- BTS interface for Studio Transmitter Link (STL)
- Supports 2K, 4K & 8K FFT sizes (modes 1, 2 & 3)
- DQPSK, QPSK, 16QAM & 64QAM modulation schemes
- Auxiliary channel (AC) input port
- Microprocessor controllable
- Single DDR2 SDRAM interface
- 1, 2, 4, 8, 16 & 32 time-interleaver depths
- 1/2, 2/3, 3/4, 5/6 & 7/8 code rates
- 1/4, 1/8, 1/16 & 1/32 guard intervals
- Time windowing reduces effects of OFDM symbol discontinuities
- Test-mode traffic generator
- Fully synchronous design
- Transmission bandwidth depends on system clock
  - 6MHz: 4096/63 = 65.01587... MHz
  - 7MHz: 2048/27 = 75.85185... MHz
  - 8MHz: 16384/189 = 86.68783... MHz
- Flexible input stream configuration
  - Single BTS input, or
  - Combined TS input with layer mapping, or
  - Individual TS input for each layer
  - Separate clocks for each TS stream
- Suitable for Xilinx FPGA only (needs Xilinx FFT core generated in Xilinx CoreGen)
- Other FPGA & ASIC vendors supported on request
- Hardware evaluation board (available extra)

ISDB-T Modulator Core

Additional Products

Zaltys Related Cores

The Zaltys 3-Layer ISDB-T demodulator (ISDBT-D) is an efficient, high-performance, ARIB STD-B31 compliant ISDB-T demodulator and is the natural partner for the Zaltys 3-Layer ISDB-T modulator core.

Zaltys MPE adapters enable Ethernet and other data services to be connected to our range of modulators and demodulators to provide high data rate communication links. The Zaltys MPE Encapsulator core (MPE-E) encapsulates high rate Ethernet and arbitrary data streams in a transport stream so they can be input to a modulator (such as the Zaltys ISDBT-M) for transmission. At the receiver, a demodulator (such as the Zaltys ISDBT-D) recovers the transport stream and the Zaltys MPE Decapsulator core (MPE-D) recreates the original Ethernet and other data streams.

Silicon Infusion also supplies many other communications-related cores to help complete your design, including our High Data Rate modulator and demodulator cores (HDRM range), DVB-S and DVB-S2 solutions and Intelsat related framing and FEC solutions. Please contact us with your enquiry.

Zaltys Evaluation Boards

Evaluation boards are available for Zaltys products including the ISDBT-M core. They connect to a PC via a USB or serial port, allowing easy communication with the ZEDwire Communicator software.

Zaltys GUI Software (ZEDwire Communicator)

ZEDwire Communicator is a software GUI which runs under Microsoft Windows®. It interacts with the Zaltys evaluation boards, enabling rapid testing and evaluation of Zaltys cores.

About Silicon Infusion and Zaltys

Silicon Infusion has been established for over ten years, and has a successful history of providing unique and innovative technical solutions to the wireless telecommunications industry. Our global client list includes organisations from many diverse market sectors - from Broadcast and Telecoms equipment manufacturers to Military solutions providers.

The Zaltys range of products are used for efficient high-speed transmission of voice, video and data. Zaltys modem cores are currently being used in many third-party products, carrying many thousands of user connections on a daily basis.

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