ISDB-T Demodulator Core

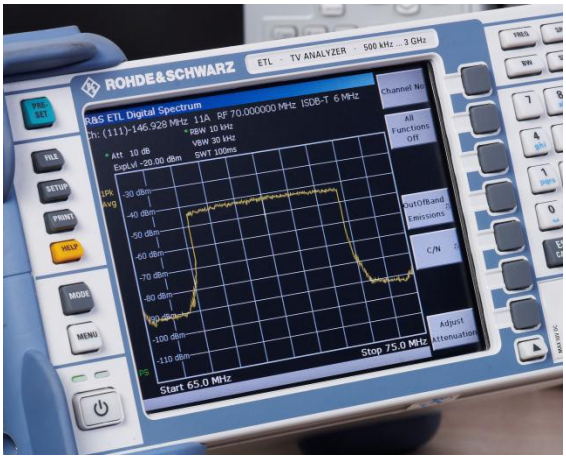
ISDBT-D

Introduction

The Zaltys ISDBT-D IP core is a 3-layer ISDB-T hierarchical demodulator compatible with the ARIB STD-B31 standard for Terrestrial Integrated Services Digital Broadcasting. The core connects to an RF frontend via one or two ADCs (real or complex baseband) and performs the necessary processing to recover 3 separate transport streams carried on 3 separate layers within an ISDB-T broadcast channel. Sophisticated error-correction and channel equalisation techniques ensure excellent performance whilst ready access to error-rate metrics allows real-time system operation to be monitored and optimised.

The demodulator provides fully automatic detection of received signal parameters and can be configured to search across any combination of ISDB-T transmission modes, guard intervals, and bandwidth settings. Modulation parameters are extracted from the embedded Transmission and Multiplexing Configuration Control (TMCC) channel and used to dynamically configure the demodulator without the need for any intervention from the host microprocessor.

A test data capture facility at points along the signal chain and a flexible microprocessor interface aids easy integration with your system. The design is available now as an efficient implementation for Xilinx FPGAs. Other FPGA's and ASICs can also be supported on request.



Typical ISDB-T Spectrum

Features

- Full 13-segment ISDB-T demodulator
- ARIB STD-B31 compliant supporting 1, 2 or 3-layers
- High-performance demodulation engine for demanding applications
- Sophisticated channel impairment correction
- Extensive error metrics
- Data capture facility at multiple points in the signal chain
- Simple microprocessor interface (SMPI)
- Available now for Xilinx FPGA

Tokyo's NTC Tower

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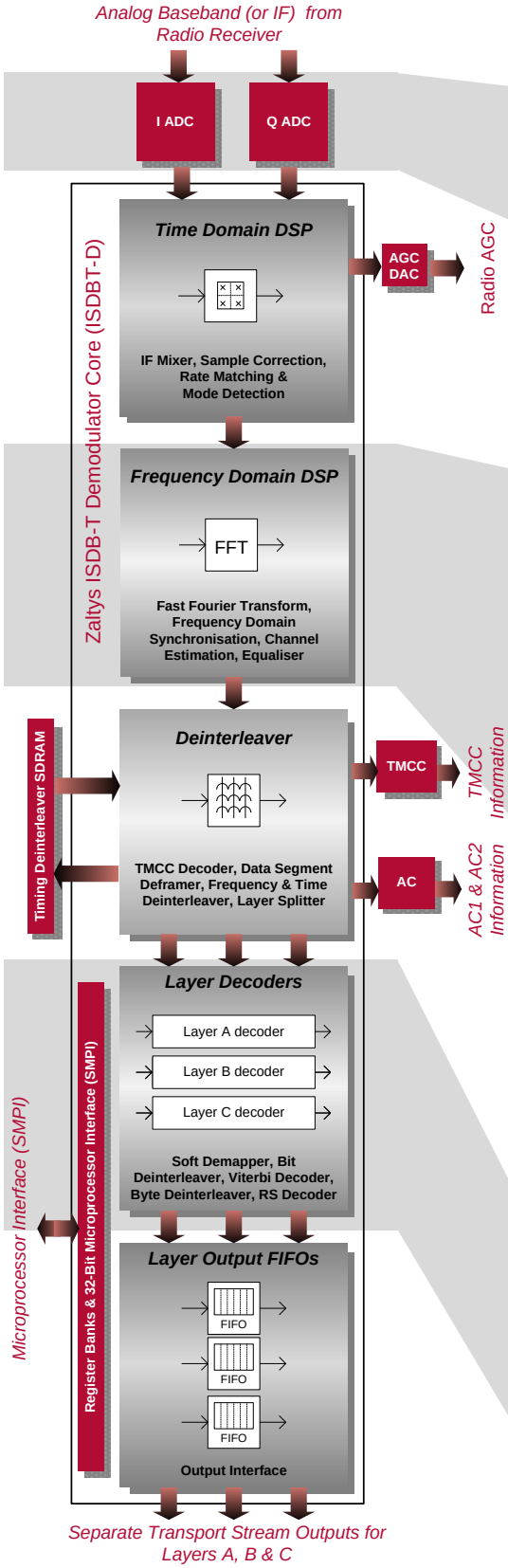


Technical Overview

COFDM Demodulator

I and Q samples of the received baseband signal need to be provided by two ADCs connected to the RF front end. Alternatively, a single ADC may be used to digitise a real-mode signal and the integrated IF mixer will convert to baseband I & Q samples.

The **Time Domain DSP** block synchronises the demodulator to the transmitter's carrier frequency, FFT sample rate, symbol and frame boundaries. The block corrects I/Q imbalance and DC offset as well as handling the interface to an RF front-end AGC circuit. The ISDB-T transmission mode, guard interval length, modulation bandwidth and sample timing are determined using autocorrelation techniques.

The Frequency Domain DSP block converts the time domain symbol data to an orthogonal frequency domain representation using a Fast Fourier Transform. The FFT sample rate depends on the ISDB-T transmission channel bandwidth as shown in Table 1. Any offset on the carrier is detected and feedback is sent to the Time Domain DSP to cancel it. Pilots, TMCC data and auxiliary channel carriers are identified and multiplex frame boundaries recognised. The post-FFT COFDM signal is analysed to estimate the impairments present on each carrier, which are used to set up per-carrier equaliser coefficients and to provide channel metrics to the downstream Viterbi decoder.

Backend 3-Layer ISDB-T Processor

The **Deinterleaver** block contains a frequency deinterleaver, performing inter-segment deinterleaving and intra-segment carrier rotation and randomisation, and a timing deinterleaver to reverse the interleaving applied by the modulator. It also contains the Data Segment Deframer which accepts raw carrier data and associated confidence levels from the COFDM demodulator and removes pilot tones, TMCC and AC channels, leaving the layer-data to pass to downstream components. A TMCC decoder block computes a weighted average of TMCC data bits from all segments in order to recover the 204-bit TMCC data.

Deinterleaved data is assigned to its appropriate layer (A, B or C) and undergoes separate processing in its own **Layer Decoder** block. Each block comprises a Soft Demapper (using Log-Likelihood-Ratio techniques), Bit Deinterleaver, Viterbi Decoder, Byte Deinterleaver and Descrambler. The output of each Layer Decoder Block is corrected by a Reed-Solomon decoder to generate the final transport stream data.

The data comprising each of the three transport streams is admitted to a separate **Layer Output FIFO** for further external downstream processing. Transport packets may be output in 188 or 204-byte format.

Table 1 : FFT Sample Rates

Transmission Bandwidth	FFT sample rate
5 MHz	6.772 MHz
6 MHz	8.127 MHz
7 MHz	9.481 MHz
8 MHz	10.836 MHz

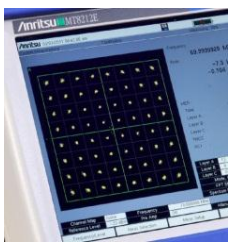
Deliverables

There are three licensing models for this IP core (each with a royalty-free and a royalty-based variant):

- Single-Project Netlist (project-based, Xilinx-specific)
- Multi-Project Netlist (site-based, Xilinx-specific)
- Multi-Project VHDL (site-based, source-code)

Deliverables	
Design Formats	Xilinx technology specific netlist VHDL source (source-code licences only)
Documentation	Hardware & programming guide
Constraints	FPGA constraints guide file
Verification	VHDL verification testbench
Templates	VHDL & verilog instantiation templates

Support
3 months support included



Typical 64QAM ISDB-T Constellation

Applications

- Professional ISDB-T receivers
- High-end consumer ISDB-T receivers
- PC-based ISDB-T receivers
- Professional broadcast test and measurement equipment
- TV head end, up-link and down-link equipment
- Multi-Dweller Unit and residential distribution equipment
- Point-to-point hierarchical communications

Full Feature List

- Full 13-segment ISDB-T demodulator, supporting 1, 2 or 3 (hierarchical) layers and compliant with the ARIB STD-B31 standard
- Auto-detection of mode, guard-interval and bandwidth
- Sophisticated channel impairment correction algorithms & per-carrier equalisation ensure excellent performance
- Support for single and dual ADC input schemes
- Three separate transport-stream outputs, one for each layer, via output FIFOs
- Extensive error metrics (including BER, MER and PER) available via register interface
- Data capture facility at multiple points through the signal chain together with PRBS data decoder aids system integration and link performance measurements
- Supports 2K, 4K & 8K FFT sizes (modes 1, 2 & 3)
- DQPSK, QPSK, 16QAM & 64QAM demodulation schemes
- 1, 2, 4, 8, 16 & 32 timing interleaver depths
- 1/2, 2/3, 3/4, 5/6 & 7/8 code rates
- 1/4, 1/8, 1/16 & 1/32 guard intervals
- A single external SDRAM device is required for time-deinterleaving. DDR1 and DDR2 devices are both supported. The design has been qualified against the Micron MT46V32M16 and MT47H32M16 devices
- Microprocessor controllable via SMPI interface (easily adapted to SPI or ARM AMBA format)
- Fully synchronous design, typically using a fixed 100MHz system clock
- Available now for Xilinx FPGA. Note that some Xilinx IP library functions are used in the design requiring an appropriate Xilinx licence. Other FPGA & ASIC vendors supported on request
- Hardware evaluation board (available extra)

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Additional Products

Zaltys Related Cores

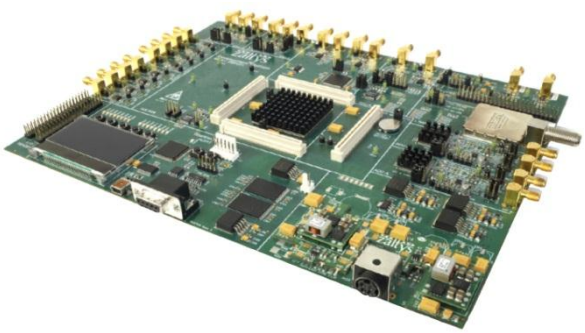
The Zaltys 3-Layer ISDB-T Modulator (ISDBT-M) is an efficient, high-performance, ARIB STD-B31 compliant ISDB-T modulator and is the natural partner for Zaltys 3-Layer ISDB-T Demodulator (ISDBT-D) core.

Zaltys MPE adapters enable Ethernet and other data services to be connected to our range of modulators and demodulators to provide high data rate communication links. The Zaltys MPE Encapsulator core (MPE-E) encapsulates high rate Ethernet and arbitrary data streams in a transport stream so they can be input to a modulator (such as the Zaltys ISDBT-M) for transmission. At the receiver, a demodulator (such as the Zaltys ISDBT-D) recovers the transport stream and the Zaltys MPE Decapsulator core (MPE-D) recreates the original Ethernet and other data streams.

Silicon Infusion also supplies many other communications-related cores to help complete your design, including our High Data Rate modulator and demodulator cores (HDRM range), DVB-S and DVB-S2 solutions and Intelsat related framing and FEC solutions. Please contact Silicon Infusion with your enquiry.

Zaltys Evaluation Boards

Evaluation boards are available for Zaltys products including the ISDBT-D core. They connect to a PC via a USB or serial port, allowing easy communication with the ZEDwire Communicator software.



Zaltys GUI Software (ZEDwire Communicator)

ZEDwire Communicator is a software GUI which runs under Microsoft Windows®. It interacts with the Zaltys evaluation boards, enabling rapid testing and evaluation of Zaltys cores.

About Silicon Infusion and Zaltys

Silicon Infusion has been established for over ten years, and has a successful history of providing unique and innovative technical solutions to the wireless telecommunications industry. Our global client list includes organisations from many diverse market sectors - from Broadcast and Telecoms equipment manufacturers to Military solutions providers.

The Zaltys range of products are used for efficient high-speed transmission of voice, video and data. Zaltys modem cores are currently being used in many third-party products, carrying many thousands of user connections on a daily basis.

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