High Data Rate Modulator Core HDRM-M

Introduction

The Zaltys High Data Rate Modulator (HDRM-M) IP core efficiently realizes the digital baseband section of a high performance modem transmit path, including symbol mapping, matched filtering, sample interpolation, and DAC interfacing. Using sophisticated DSP techniques, the core can generate almost any modulation scheme up to 8 bits wide, such as (but not restricted to) BSPK, QPSK, offset-QPSK, 8/16/32/64/128/256QAM, 16/32APSK, and various "non-square" (NS) schemes, all to a high performance level and at high symbol rates. The modulator is highly flexible, supporting continuously variable software-selectable symbol rates of between 2.5 kbaud and 40Mbaud, when operating with a fixed 100MHz system/DAC clock rate. This is the typical performance achievable when implementing the design using inexpensive FPGA devices, but increased data rates are possible by targeting the design to higher performance FPGA families which allow an increase in system clock rate. Once configured via the 32-bit microprocessor interface, the modulator operation is completely automatic .
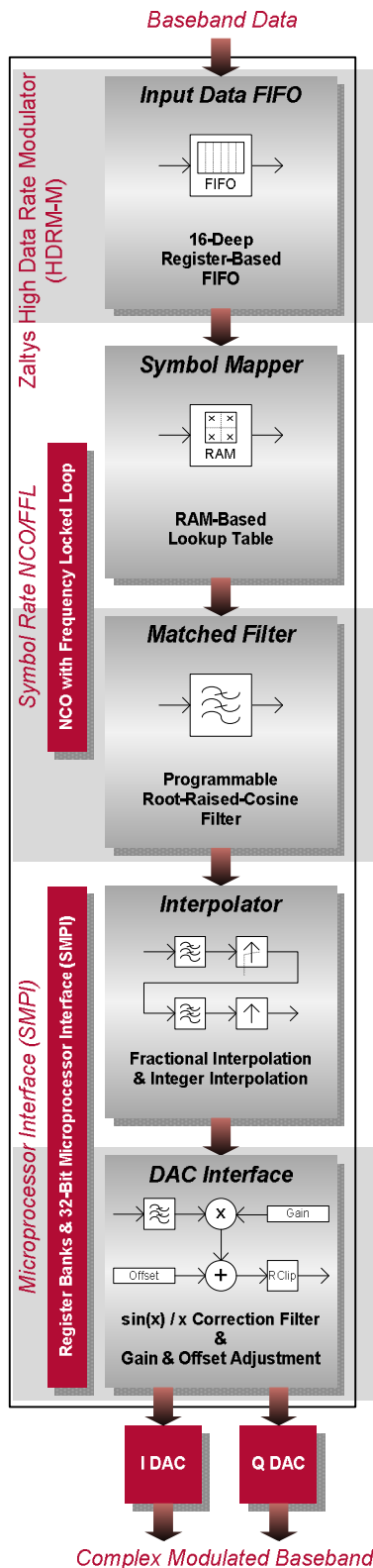
Applications

The HDRM-M core is ideally suited to point-to-point wireless applications such as satellite communications and microwave line-of-sight backhaul links (e.g. for cellular, broadband or WiMAX). It also has applications in wired and optical links.

Features

" Versatile digital modulation engine

" Programmable constellation mapper supports multiple constellations from BPSK to 256QAM

" Supports offset-QPSK (OQPSK)

" Supports continuously variable symbol rates

" Internal filter interpolates up to a factor of 8192

" Supports typical rates of 2.5 kbaud to 40Mbaud with 100MHz clock (range scales linearly with clock frequency)

" Integrated transmit symbol rate NCO

" FLL (frequency-locked-loop) allows transmit symbol rate to be locked to an external reference

" Matched filter with fully programmable alpha from 20% upwards

" Programmable 2's complement or offset-binary 8, 10, 12 or 14- bit DAC I & Q interfaces

" Versatile FIFO input accepts n-bit symbols (1 $\leq n \leq 8$) or raw I / Q constellation point coordinates

" Built- in $\sin(x)/x$ DAC compensation filters and internal gain and offset calibration

" Highly configurable and versatile - fully programmable via simple microprocessor interface (SMPI)

" Suitable for FPGA or ASIC implementation

" Xilinx Virtex® - 6 implementations support over 100Mbaud (800Mb/s throughput) with 256QAM

" Synchronous design with single clock

" Hardware evaluation board (available extra)

High Data Rate Modulator Core

Baseband Data

Zaltys High Data Rate Modulator (HDRM-M)

Input Data FIFO

FIFO

16-Deep
Register-Based
FIFO

Symbol Mapper

RAM

RAM-Based
Lookup Table

Matched Filter

Programmable
Root-Raised-Cosine
Filter

Interpolator

Fractional Interpolation
& Integer Interpolation

DAC Interface

Gain

Offset — R Clip

sin(x) / x Correction Filter
&
Gain & Offset Adjustment

Symbol Rate NCO/FFL

NCO with Frequency Locked Loop

Microprocessor Interface (SMPI)

Register Banks & 32-Bit Microprocessor Interface (SMPI)

I DAC   Q DAC

Complex Modulated Baseband

Technical Overview

Raw data is mapped to I and Q constellation points by the mapper. Alternatively, the modulator can be supplied directly with the I and Q constellation points. The mapped symbols are then passed through a programmable matched filter, before being interpolated up to the DAC sample rate. A built-in FLL allows the symbol rate to be locked to an external reference.

The modulator data path consists of five distinct datapath sections. These correspond to the Input Data FIFO, Symbol Mapper, Matched Filter, Interpolator and DAC Interface functions. System timing is controlled by an integrated Symbol Rate NCO/FLL. Communications with the core is handled by a 32-bit Simple Microprocessor Interface (SMPI).

Input Data FIFO

This block provides a small sixteen word input FIFO for accepting transmit data, either in the form of n-bit symbols ($1 \leq n \leq 8$) or raw I/Q constellation points.

Symbol Mapper

This block maps symbol inputs to I and Q constellation points using a RAM based look-up table, which is fully programmable via the microprocessor interface. It supports a huge set of modulation schemes, including offset-QPSK and asymmetrical schemes (such as NS-nQAM).

Matched Filter

Mapped symbols are passed through an RRC filter, which can support excess bandwidths of 20% or greater. It is fully programmable via the microprocessor interface.

Interpolator

This block matches the data to the DAC conversion rate, by using a fractional interpolation filter followed by an integer interpolation filter, up to a factor of 8192.

DAC Interface

The modulated output can be gain and offset calibrated, and a DAC compensation filter is available to compensate for sin(x) / x roll-off. The final output takes the form of I and Q sample pairs suitable for passing to high conversion rate 8, 10, 12 or 14 bit DACs.

Symbol Rate NCO/FLL

This block controls the rate of data flow through the modulator. The Symbol Rate NCO can be configured as a free-running, or can be locked to an external reference signal using the Symbol Rate FLL.

Simple Microprocessor Interface (SMPI)

This block controls the microprocessor interface to the modulator register set. It utilizes a conventional single transaction DTREQ/DTACK handshake protocol.

Deliverables

There are four licensing models for this IP core (each with a royalty-free and a royalty-based variant):

" Single-Project Netlist (project-based, FPGA-specific)

" Multi-Project Netlist (site-based, FPGA-specific)

" Multi-Project VHDL (site-based, source-code)

" Multi-Project VHDL & C (site-based, full-capability)

The "full-capability" option provides all the VHDL source code, C models and MATLAB® models. It also includes additional documentation which details the algorithms used in the design, allowing fine tuning of system performance. FPGA-specific netlists are available for multiple vendors, including Xilinx, Altera and Lattice.

| Deliverables	
Documentation	Hardware guide
	Programming guide
	Simulation guide
	Architectural overview*
	Advanced programming guide*
	Full capability licence only
Design Formats	Technology specific netlist
	VHDL source*
	MATLAB® Model**
	Source & full capability licences
	**Full capability licence only*
Constraints	FPGA constraints guide file
Verification	VHDL verification testbench
Templates	VHDL & verilog instantiation templates

Support
3 months support included

Additional Products

Zaltys Related Cores

The Zaltys High Data Rate Demodulator (HDRM-D) IP core forms the digital baseband section of a high performance modem receive path, including quasi-zero IF to baseband conversion, sample decimation, symbol timing recovery, and carrier recovery. The core can demodulate BPSK, QPSK, offset-QPSK (OQPSK), 8PSK and 16QAM, all to a high performance level and at high symbol rates. The Zaltys High Data Rate Enhanced Demodulator (HDRM-D2) IP core adds support for 8/32/64 QAM & 16/32 APSK, and comes with an integral blind adaptive equaliser. It also supports an increase in data path resolution up to 14-bits, allowing it to cope with higher levels of adjacent channel interference.

Zaltys MPE adapters enable Ethernet and other data services to be connected to our range of modulators and demodulators to provide high data rate communication links. The Zaltys MPE Encapsulator core (MPE-E) encapsulates high rate Ethernet and other arbitrary data streams in a transport stream so they can be input to a modulator (such as the Zaltys HDRM-M) for transmission. At the receiver, a demodulator (such as the Zaltys HDRM-D) recovers the transport stream and the Zaltys MPE Decapsulator core (MPE-D) recreates the original data stream.

Silicon Infusion also supplies many other communications-related cores to help complete your design, including our High Data Rate modulator and demodulator cores (HDRM range), DVB-S and DVB-S2 solutions and Intelsat related framing and FEC solutions. Please contact us with your enquiry.
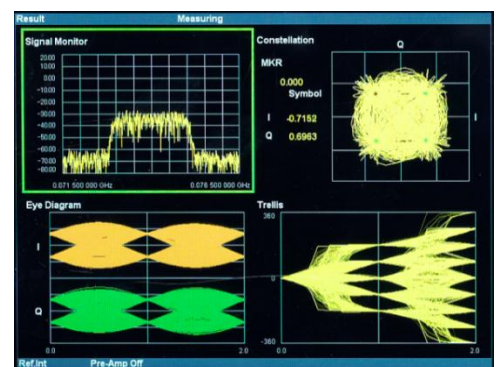
High Data Rate Modulator Core
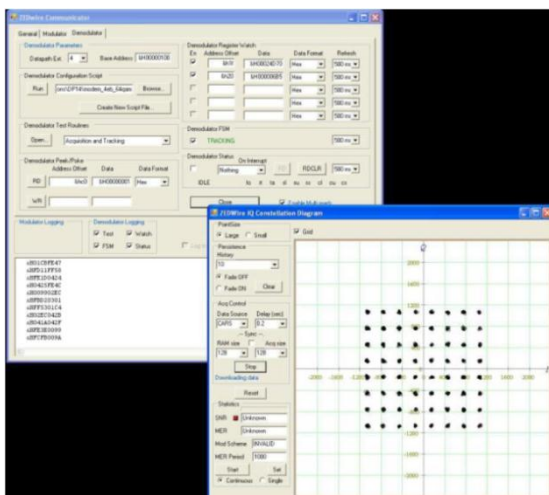
Zaltys Evaluation Boards

Evaluation boards are available for Zaltys products including the HDRM-M core. They connect to a PC via a USB or serial port, allowing easy communication with the ZEDwire Communicator software.
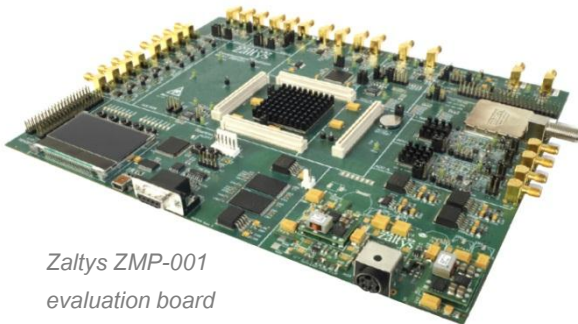
Zaltys ZMP-001 evaluation board

About Silicon Infusion and Zaltys

Silicon Infusion has been established for over ten years, and has a successful history of providing unique and innovative technical solutions to the wireless telecommunications industry. Our global client list includes organisations from many diverse market sectors - from Broadcast and Telecoms equipment manufacturers to Military solutions providers.

The Zaltys range of products are used for efficient high-speed transmission of voice, video and data. Zaltys modem cores are currently being used in many third-party products, carrying many thousands of user connections on a daily basis.

Zaltys GUI Software (ZEDwire Communicator)

ZEDwire Communicator is a software GUI which runs under Microsoft Windows®. It interacts with the Zaltys evaluation boards, enabling rapid testing and evaluation of Zaltys cores.

ZEDwire Communicator Software

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