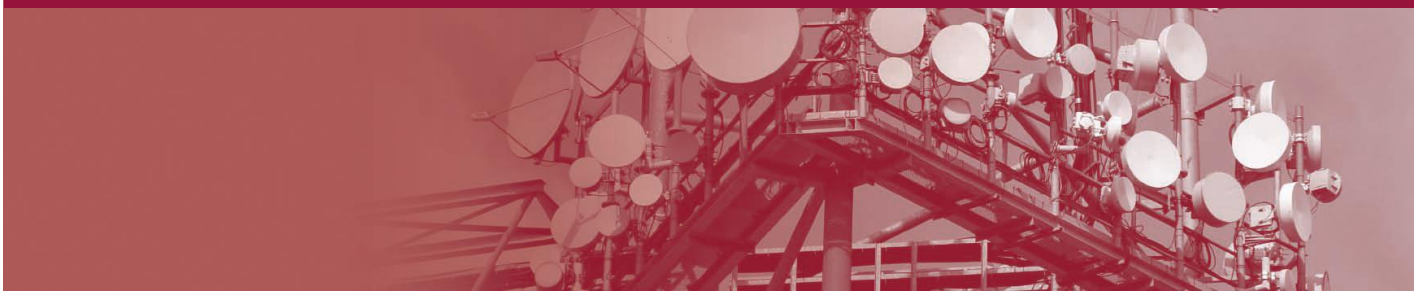
High Data Rate Enhanced Demodulator HDRM-D2

Product Overview



Features

- Versatile digital demodulation engine for BPSK, QPSK, offset-QPSK (OQPSK), 8PSK, 8QAM (3 shapes), 16QAM, 64QAM, 16APSK & 32APSK
- Close to theoretical performance
- Option to increase datapath resolution to help cope with elevated levels of adjacent carrier interference
- N-stage symbol rate blind adaptive equaliser option reduces linear channel distortions such as multipath
- Supports continuously variable symbol rates
  - Internal filter decimates up to a factor of 4096
  - Supports typical rates of 4.9kbaud to 40Mbaud with 100MHz clock (range scales linearly with clock)
- Four matched filter configurations with alphas of 0.2, 0.25, 0.35 & 0.4 (others available on request)
- Fast acquisition algorithm
  - Combined coarse/fine frequency scan
  - High probability of first pass acquisition
- Highly configurable and versatile
  - Fully programmable via microprocessor interface
  - Independent acquisition & track parameters
  - Configurable timing & carrier lock characteristics
- 10 to 14-bit I & Q datapath/ADC interface resolution
- Constellation output interface suitable for connecting to soft-decision forward error correction (FEC)
- AGC control interface to analogue front-end
- Status interface reports real-time demodulation state
- Simple microprocessor interface (SMPI)
- Comes with software driver in C
- Extensive support for software monitoring
- Suitable for FPGA or ASIC implementation
- Synchronous design with single clock
- Hardware evaluation board (available extra)

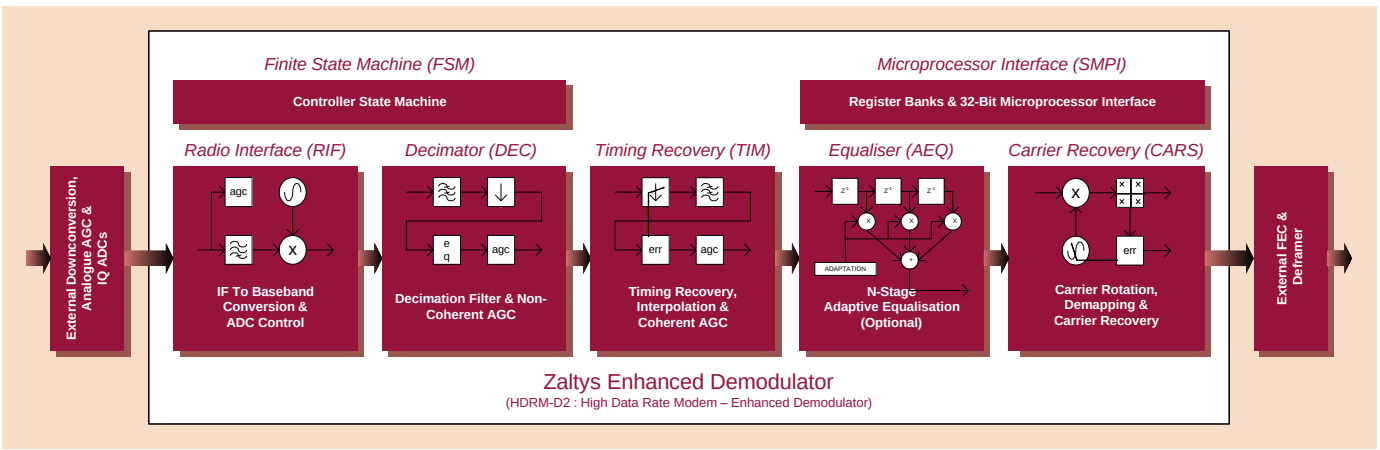
Introduction

The Zaltys High Data Rate Enhanced Demodulator (HDRM-D2) IP core efficiently realizes the digital baseband section of a high performance modem receive path, including quasi-zero IF to baseband conversion, sample decimation, symbol timing recovery, blind adaptive equalisation, and carrier recovery. Using sophisticated DSP techniques, the core can demodulate BPSK, QPSK, offset-QPSK (OQPSK), 8PSK, 8QAM (3 shapes), 16QAM, 64QAM, 16APSK and 32APSK modulation schemes, all to a high performance level and at high symbol rates. The demodulator is highly flexible, supporting continuously variable software-selectable symbol rates of between 4.9kbaud and 40Mbaud, when operating with a fixed 100MHz system/ADC clock rate.

The HDRM-D2 core is ideally suited to point-to-point wireless applications such as satellite communications and microwave line-of-sight backhaul links (e.g. cellular, broadband or WiMAX). It also has applications in wired and optical links.

Technical Overview

In order to deliver performance close to the theoretical limits, the design utilizes multiple gain control stages within the data path to maximize dynamic range. Up to four sets of matched root-raised cosine filter coefficients can be incorporated into a given implementation, allowing four excess bandwidth values for the input signal to be selected in software. All aspects of the timing and carrier recovery are fully programmable, including loop filter coefficients and lock detector thresholds. In addition, monitoring registers provide a high degree of software visibility for parameters such as frequency offsets, lock levels and SNR estimation. The primary



High Data Rate Enhanced Demodulator HDRM-D2

Product Overview

Technical Overview continued

demodulator output is a sequence of symbols, nominally positioned at the specified constellation points. This allows a soft-decision forward-error-correction function to be easily used with this demodulator. Additional outputs include an I & Q monitor feature, which can be used to either view the constellation (via an external DAC), or alternatively, to carry hard-sliced data.

Demodulator Architecture

The demodulator datapath consists of six distinct sections. These correspond to the Radio Interface, Decimator, Timing Recovery, Adaptive Equaliser and Carrier Recovery functions. The overall operation of the system is automatically managed by an integrated Finite State Machine controller. Communications with the core is handled by a 32-bit Simple Microprocessor Interface.

Radio Interface (RIF)

This block converts from quasi-zero IF to baseband and, in conjunction with a suitable gain-programmable input stage, drives the front-end analogue AGC. It also has circuitry for eliminating DC offsets and IQ imbalances.

Decimator (DEC)

This block may be programmed to provide sample-rate decimation factors of between 1 and 4096, in octave steps.

Timing Recovery (TIM)

This block uses an interpolating filter to resample the input signal at the symbol rate. This resampled input is then filtered using a root raised cosine matched filter.

Blind Adaptive Equaliser (AEQ)

This optional block uses an N stage ($3 \leq N \leq 15$) linear transversal filter to significantly reduce the effect of certain channel induced distortions, such as multipath.

Carrier Recovery (CARS)

This block implements carrier recovery, carrier rotation and coherent gain functions, so that the incoming symbol points fall on the nominal constellation points.

Finite State Machine (FSM)

This block controls the demodulator and schedules the procedures for acquisition, tracking, and reacquisition.

Simple Microprocessor Interface (SMPI)

This block controls the microprocessor interface to the demodulator register set. It utilizes a conventional single transaction DTREQ/DTACK handshake protocol.

Deliverables

There are four licensing models for this IP core:

- Single-Project Netlist (project-based, FPGA-specific)
- Multi-Project Netlist (site-based, FPGA-specific)
- Multi-Project VHDL (site-based, source-code)
- Multi-Project VHDL & C (site-based, full-capability)

The "full-capability" option provides all the VHDL source code, C models and MATLAB® models. It also includes additional documentation which details the algorithms performance. Site based licenses can be used in multiple projects. FPGA-specific netlists are available for multiple vendors, including Xilinx, Altera and Lattice.

Deliverables	
Documentation	Hardware Guide Programming Guide Simulation Guide Architectural Overview* Advanced Programming Guide* **full capability licence only*
Design Formats	Technology Specific Netlist VHDL Source* MATLAB® Model** **source & full capability licences* ***full capability licence only*
Constraints	FPGA Constraints Guideline File
Verification	VHDL Testbench
Templates	VHDL & verilog Instantiation Templates
Additional Items	Software Driver in C Analogue Interfacing Application Note
Support	
3 Months Support Included	

Additional Products

Zaltys Evaluation Board (ZMP-001)

This board is designed to demonstrate Zaltys products, including the HDRM-D, at rates of over 65Mbaud. The board uses Xilinx Virtex-4 technology, and can be fitted

with custom daughterboard's to extend its functionality. It connects to a PC via a USB or serial port, allowing easy communication with the ZEDcommunicator software.

Zaltys ZMP-001 GUI Software (ZEDwire Communicator)

ZEDwire Communicator is a software GUI which runs under Microsoft Windows®. It interacts with the ZMP-001 board, allowing rapid evaluation of Zaltys cores.

Related Cores

The Zaltys High Data Rate Demodulator (HDRM-D) core is similar to the HDRM-D2, but with a fixed 10-bit datapath resolution. It supports BPSK, QPSK, OQPSK, 8PSK, and 16QAM modulation schemes, with no adaptive equaliser.

The Zaltys High Data Rate Modulator (HDRM-M) core forms the digital baseband section of a high performance modem transmit path, including symbol-mapping, matched-filtering, interpolation, and DAC interfacing.

Silicon Infusion also supplies many other related cores to help complete your design, such as DVB and Intelsat related framing and FEC solutions. Please contact Silicon Infusion with your enquiry.

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